What is claimed is:

[Claim 1] 1. A charge pump comprising:

an up input and a down input to the charge pump;
an output having an output capacitance to be charged in response to the up input and discharged in response to the down input;
a fixed current source that sources a relatively constant source current to a first junction node;
a variable current source that sources a varying source current to a second junction node, wherein the varying source current varies in response to a control voltage;
a first driver transistor, coupled to conduct current between the first junction node and the output in response to the up input;
a second driver transistor, coupled to conduct current between the second junction node and the output in response to the down input;
a first series transistor, coupled to conduct current between the first junction node and an intermediate node in response to an inverse of the up input;
a second series transistor, coupled to conduct current between the second junction node and the intermediate node in response to an inverse of the down input;
a sampling capacitor for storing a sampled charge, generating the control voltage to the variable current source; and
a sampling switch coupled to conduct current between the intermediate node and the sampling capacitor when the up input and the down input are inactive, whereby the intermediate node is coupled to the sampling capacitor to adjust the varying source current.

[Claim 2] 2. The charge pump of claim 1 wherein the sampling switch comprises a sampling transistor and a logic gate;

wherein the sampling transistor receives a logic output signal on a gate;

wherein the logic gate receives the up input and the down input or the inverse of the up input and the inverse of the down input and generates the logic output signal.

[Claim 3] 3. The charge pump of claim 1 wherein the sampling switch comprises a first sampling transistor and a second sampling transistor in series between the intermediate node and a control node of the sampling capacitor;

wherein the first sampling transistor receives the inverse of the up input on a gate;
wherein the second sampling transistor receives the inverse of the down input on a gate.

[Claim 4] 4. The charge pump of claim 3 wherein the first sampling transistor is an n-channel transistor;

wherein the second sampling transistor is an n-channel transistor.

[Claim 5] 5. The charge pump of claim 4 wherein the first driver transistor is a p-channel transistor;

wherein the first series transistor is a p-channel transistor;
wherein the second driver transistor is an n-channel transistor; and
wherein the second series transistor is an n-channel transistor.

[Claim 6] 6. The charge pump of claim 5 wherein the up input is pulsed low to charge the output capacitance;

wherein the down input is pulsed high to discharge the output capacitance.

[Claim 7] 7. The charge pump of claim 6 further comprising:

a loop filter that includes the output capacitance charged and discharged by the charge pump;

a phase comparator, receiving a feedback clock and a reference clock, for generating the up input and the down input in response to phase comparisons;
a voltage-controlled oscillator (VCO) sensing an output voltage on the output capacitance and generating the feedback clock with a frequency dependent on the output voltage.

[Claim 8] 8. The charge pump of claim 7 wherein the up input is high and the down input is low for idle periods of time between phase comparisons by the phase comparator in a phase-locked loop (PLL);

wherein the intermediate node is sampled during the idle periods of time.

[Claim 9] 9. The charge pump of claim 8 wherein the up input is low and the down input is high simultaneously during a locked period when the PLL is stable and phase comparison of a feedback clock to a reference clock detects no phase difference;

wherein both the first and second driver transistors are on during the locked period.

[Claim 10] 10. The charge pump of claim 3 wherein the variable current source comprises:

a first sink transistor, receiving a first voltage bias on a gate;
a second sink transistor, receiving the control voltage on a gate;
wherein the first sink transistor and the second sink transistor are in series between the second junction node and a ground.

[Claim 11] 11. The charge pump of claim 10 wherein the first and second sink transistors are n-channel transistors.

[Claim 12] 12. The charge pump of claim 11 wherein the fixed current source comprises:

a first source transistor, receiving a second bias voltage on a gate;
a second source transistor, receiving a third bias voltage on a gate;
wherein the first source transistor and the second source transistor are in series between the first junction node and a power supply.

[Claim 13] 13. The charge pump of claim 12 wherein the first and second source transistors are p-channel transistors.

[Claim 14] 14. The charge pump of claim 13 further comprising:

a bias generator for generating the second bias voltage, the bias generator comprising a first bias transistor, a second bias transistor, and a reference current source in series between the power supply and the ground;
wherein the first bias transistor has a gate receiving the second bias voltage;
wherein the second bias transistor has a gate receiving the third bias voltage;
wherein a node between the second bias transistor and the reference current source generates the second bias voltage.

[Claim 15] 15. The charge pump of claim 14 wherein the sampling capacitor is connected between a control node having the control voltage and the ground.

[Claim 16] 16. The charge pump of claim 15 wherein the first driver transistor and the first series transistor have a same gate size;

wherein the second driver transistor and the second series transistor have a same gate size,
whereby series transistors match driver transistors.

[Claim 17] 17. A current-adjusting charge pump comprising:

a current source, coupled between a power supply and an upper junction node;

a first driver transistor, having a gate driven by an inverse-charging signal, a source connected to the upper junction node, and a drain connected to an output;
a first series transistor, having a gate driven by a charging signal, a source connected to the upper junction node, and a drain connected to an intermediate node;
a second driver transistor, having a gate driven by a discharging signal, a source connected to a lower junction node, and a drain connected to the output;
a second series transistor, having a gate driven by an inverse-discharging signal, a source connected to the lower junction node, and a drain connected to the intermediate node;
a first switch transistor, having a gate driven by the inverse-charging signal, a drain connected to the intermediate node, and a source connected to a mid-switch node;
a second switch transistor, having a gate driven by the inverse-discharging signal, a drain connected to the mid-switch node, and a source connected to a charge-storage node;
a sampling capacitor coupled between the charge-storage node and a fixed voltage;
a fixed sink transistor having a gate driven by a bias voltage, a drain connected to the lower junction node, and a source connected to a mid-sink node; and
a variable sink transistor having a gate connected to the charge-storage node, a drain connected to the mid-sink node, and a source connected to a ground.

[Claim 18] 18. The current-adjusting charge pump of claim 17 wherein the first series transistor and the first driver transistor are p-channel transistors;

wherein the second series transistor, the second driver transistor, the first switch transistor, the second switch transistor, the fixed sink transistor, and the variable sink transistor are n-channel transistors.

[Claim 19] 19. An accurate charge pump with matched up and down currents for charging and discharging a filter capacitor on an output node, the accurate charge pump comprising:

an UP signal for charging the filter capacitor when pulsed high;
an UPB signal for charging the filter capacitor when pulsed low;
a DN signal for discharging the filter capacitor when pulsed high;
a DNB signal for discharging the filter capacitor when pulsed low;
fixed current source means for generating a fixed current to a first junction;
variable current source means for generating an adjustable current to a second junction in response to a control voltage on a control node;
first driver transistor means, responsive to the UPB signal on a gate, for conducting current from the first junction to the output node;
first series transistor means, responsive to the UP signal on a gate, for conducting current from the first junction to an intermediate node;
second driver transistor means, responsive to the DN signal on a gate, for conducting current from the second junction to the output node;
second series transistor means, responsive to the DNB signal on a gate, for conducting current from the second junction to the intermediate node;
sampling capacitor means for storing charge to generate the control voltage on the control node; and
sample switch means for conducting between the intermediate node and the control node when UPB and DNB signals are both high.

[Claim 20] 20. The accurate charge pump of claim 19 wherein the sample switch means comprises:

first switch transistor means, responsive to the UPB signal on a gate, for conducting current in a first channel;
second switch transistor means, responsive to the DNB signal on a gate, for conducting current in a second channel;
wherein the first channel and the second channel are in series between the intermediate node and the control node.

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